Influence of Manufacturing Variations in I_{DDQ} Measurements: A New Test Criterion

Juan M. Díez and Juan C. López†
Departamento de Ingeniería Electrónica. Universidad Politécnica de Madrid.
†Departamento de Informática. Universidad de Castilla-La Mancha.
e-mail: jmdiez@die.upm.es, lopez@uclm.es

Abstract

This work presents a new I_{DDQ}-based test criterion supported by the characteristics of a set of experimental testing measurements realized over different samples of industrial ICs and by the definition of the corresponding simulation model. Comparing the current consumptions of a specific circuit a significant correlation between measurements can be observed. The current behaviour can be divided into two parts: (1) a circuit dependent one, which has a major contribution, and affects equally all the devices in a given die, and (2) a smaller die dependent fraction due to variations, defective and non-defective, of each of the devices of a specific die. In this paper, a current model is defined, introducing the effects of manufacturing variations in the basic equations of the sub-threshold current to explain that double behaviour. The results show how it is possible to obtain a lot of information from I_{DDQ} measurements and how other test selection criteria can be applied to increase the I_{DDQ} testing sensitivity and quality.

1 Introduction

I_{DDQ} testing is performed by measuring the quiescent current of the power supply and comparing this obtained value with a fixed limit. In the last years this technique has proven to be very useful and has been an important contribution to improve the quality of CMOS ICs [1].

The selection of the current limit is one of the open and key questions in the utilization of I_{DDQ} testing. The selection criterion is based on a pass/fail limit and it is just efficient with failures which provoke high increments of consumption. However, the sensitivity of the I_{DDQ} is insufficient in order to determine the correctness of ICs with consumptions close to the current limit. The current limit has to be fixed as a tradeoff between the yield and the required quality, that is, it must be selected to reduce the cost impact of yield loss, without imposing a penalty on defect detection [2]. Some approaches have been proposed for a better limit selection: current estimation methodologies [3], statistical analysis of I_{DDQ} data [4][5] or the consideration of global process variations [6].

In addition, the forecast for deep sub-micron technologies shows an abrupt increment of the background current in several orders of magnitude and a decrement of some defect effects [7]. The separation between defective and non-defective currents and, therefore, the I_{DDQ} sensitivity will diminish dramatically. These problems have been detected and certain solutions have been proposed like reducing the temperature of measurements, the design partitioning or the employment of an insulated bulk [8].

In conclusion, I_{DDQ} needs a more sensitive criterion. In this work we will propose the study of the global characteristics of the quiescent current in order to define such a criterion. This should allow to detect any anomaly in the circuit consumption and not only increments of the maximal current. Experimentally, we can observe that the current consumption per test pattern for a set of samples of the same IC is repetitive. Two dice with the same manufacturing process have more common characteristics than differences and their current consumptions under the same test pattern are similar. I_{DDQ} testing is a test of the technology and it provides a global image of a die. Therefore, applying that condition, any technological anomaly will provoke an alteration in the statistical characteristics of the quiescent current distributions. More information can then be extracted and later applied for a better test preparation. To reach this goal, two main questions should be answered. First, whether there is any correlation between the distribution of the I_{DDQ} current and other parameters such as MOS device parameters, and second, whether we can define a measurement methodology to extract that information.

The work presented here concerns with the analysis of equal devices with different influences of the fabrication process tolerances. The results obtained show how any anomalous difference between an ideal die and a given die can be observed by statistical analysis. Based on this, we will improve the test sensitivity defining a new I_{DDQ} testing criterion with a really small increment of the complexity of the measurement system.

2 An experimental case

The initial point of this work is shown in Figures 1 and 2. The goal of this experiment was the analysis of the

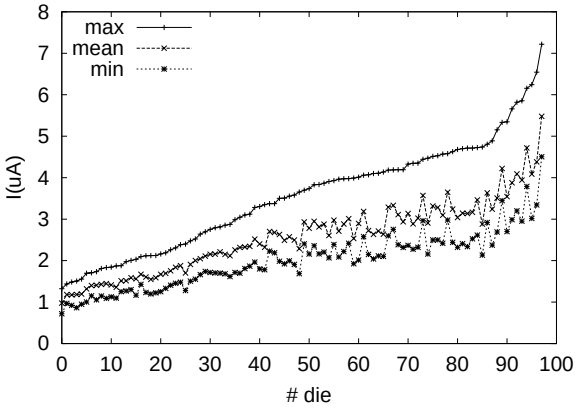

Figure 1: **Maximal, mean and minimal quiescent current per die. The x-axis is sorted by maximal currents in ascending order.**

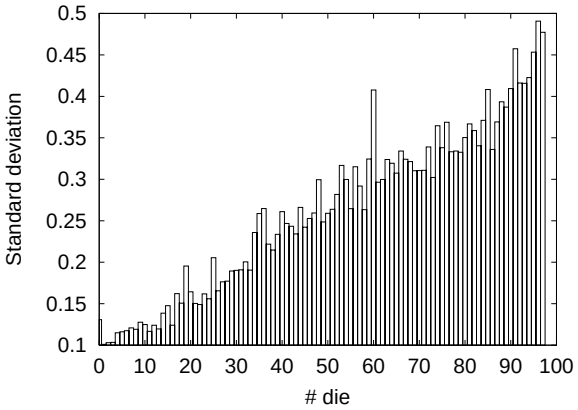

Figure 2: **Standard deviation of quiescent current per die. The x-axis is the same than fig. 1.**

I_{DDQ} current distribution of one hundred samples of a specific CMOS circuit with 250,000 transistors ($0.7\mu m$ technology), doing comparisons vector to vector and circuit to circuit[1].

Figure 1 shows the maximal, mean and minimal quiescent currents for every die and Figure 2 shows the standard deviation of their current distributions per die. The x-axis of both figures represents the number of samples and are ordered by their maximal currents.

To continue the analysis we compared the current consumptions of each die with respect to a selected die, which has been considered as a golden circuit. This method allowed to separate common current contributions from those contributions that are due to device anomalies, which can be better observed. Figures 3 and 4 show this comparison. Now, the x-axis is ordered by mean currents.

The criterion of I_{DDQ} testing uses only the maximal current to determine correct or failed circuits, but another important information can be extracted from these figures. The same general behaviour can be observed in all the dice because each of them has followed the same manufacturing process. Therefore all of them have similar technological characteristics, which implies the similar current behaviours clearly appreciated in the figures. On the other hand, the small differences between different samples are due to tolerances and variations of the manufacturing process. These differences follow a similar pattern. However, our interest is centered on why circuits with values of current far from the maximal have larger dispersions of those values (Figure 4). Thus, we can state that two different aspects contribute to the total current value: a circuit dependent one, which has a major contribution, and is a characteristic of the circuit, and a smaller die dependent one, due to manufacturing variations, defective and non-defective.

According to the data obtained from the experiment, the

[1]These circuits have been supplied by ALCATEL.

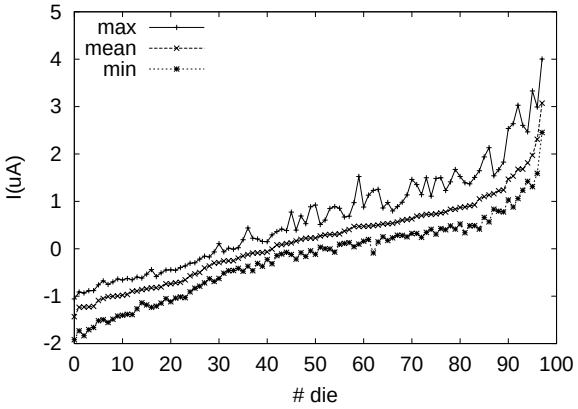

Figure 3: **Maximal, mean and minimal current differences of every die and a golden circuit. The x-axis is sorted by mean currents in ascending order.**

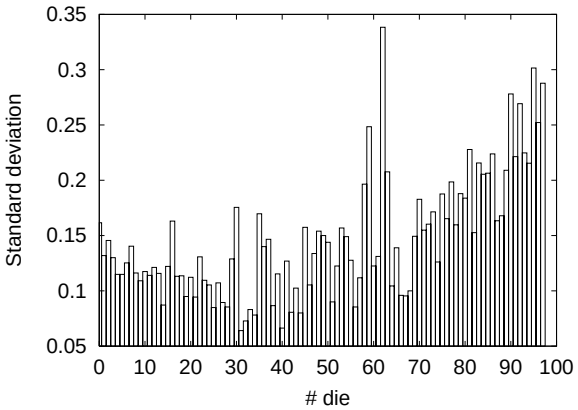

Figure 4: **Standard deviation of current differences of every die and a golden circuit. The x-axis is the same than fig. 3.**

curve of mean consumptions can be approximated by a Normal behaviour and the current distributions of each die by a combination of Normal and Log-Normal distributions. As, in general, normal distributions are due to variations following a lineal relationship and Log-Normal distributions to variations following an exponential one, a first explanation about this behaviour of the quiescent current can be found out in the different contributions to its value: the leakage current is proportional to the areas of source and drain terminals and the sub-threshold current is proportional to the exponential of the sub-threshold voltage. Next sections will analyze some of these aspects.

3 Tolerances and Manufacturing Variations

During wafer processing different operations are carried out. The fabrication tolerance provokes the apparition of deviations in the device details: variations in the thickness of either the oxide or the polisilicon layers, in the resistance of implanted layers, in the width of lithographical defined features, and in the registration of a photo-mask with respect to previous masking operations [9]. These small variations are many times critical since they affect to the device electrical characteristics.

The double behaviour commented in the previous section can be explained by a model which classifies the different causes that produce these circuit variances into two groups: inter-die variability and intra-die device mismatch [10]. Inter-die variability is characterized by die-to-die or wafer-to-wafer process variability and it affects equally to all the devices in a given die. Intra-die device mismatch is a phenomenon which causes that similarly designed transistors and under equivalent biasing conditions behave differently. The inter-die effect can be represented by a parameter mean for every die and the intra-die by a deviation in this mean of every device in this die. Variations due to inter-die variability are generally much larger than intra-die values. The relationship between inter-die and intra-die variations is shown in Figure 5.

In this work, we are going to apply this model to distributions of quiescent current consumptions, since the experimental measurements follow that double behaviour.

4 Tolerance-based Current Model

In this section we address the definition of a simple consumption model to explain experimental measurements and to study the effects of parameter variations. The quiescent current has two major components: the reverse biased p-n junction leakage current and the transistor sub-threshold leakage current. We can define a global model for the quiescent current studying the equations of both contributions

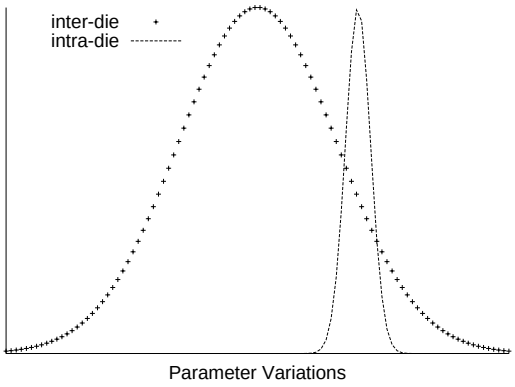

Figure 5: **Relationship between intra-die and inter-die parameter variations.**

and the variations of all their parameters. In long channel technologies, which is the case of the circuit whose measurements were presented in section 2, the quiescent current is mainly due to the reverse biased p-n junction. But upon reducing the channel length, the sub-threshold currents turn out to be the main contributions, which implies that they dominate the current behaviour in today's deep sub-micron technologies. Our work is centered on the study of these sub-threshold currents.

For an NMOS device, the quiescent current due to sub-threshold conduction [11] follows this simplified relationship:

$$I_{subth} \propto Cox\frac{W}{L}exp(-\frac{V_{th}}{\xi v_t})$$

where C_{ox} is the gate capacitance per unit area, W is the channel width, L is the channel length and V_{th} is the sub-threshold voltage. These four parameters are affected by their tolerance, therefore, we need to know their distributions and their correlations. Anyway, this equation is dominated by V_{th} variations due to exponential relation between V_{th} and I_{subth}.

Due to this fact, we can make a simplification based in considering just the contribution of the sub-threshold current and the influence of just one parameter, the sub-threshold voltage, V_{th}. The obtained results validates this simplification, since they keep the consumption behaviour shown by the experimental measurements. This approach will allow to better explain the concepts and the influences of parameter variations, making unnecessary the use of more complete (and complex) models.

4.1 Simple Current Model

In this simple model, the current of an NMOS device affected by the variation of V_{th} is given by:

$$I_{subth} = I_{typical}exp(-\frac{\triangle V_{th}^{inter} + \triangle V_{th}^{intra}}{\xi v_t})$$

where $I_{typical}$ is the consumption of a typical transistor and $\triangle V_{th}^{inter}$ and $\triangle V_{th}^{intra}$ are the variations of sub-threshold voltage due to inter-die and intra-die tolerances, respectively. These variations can be approximated by a Normal distribution. This, together with the exponential function of the previous equation, explains the Log-Normal consumption contribution of each die found in the real measurements commented in section 2.

Standard deviations of parameter distributions can be estimated using the parameters provided by the manufacturers (SPICE parameters), and then, used in a Monte Carlo analysis to calculate values of parameter variations for every transistor and every gate.

4.2 Simulation Model.

In CMOS design, there is no current flow from one stage to another due to the MOS gate capacitance. Under these isolation circumstances, the global quiescent current will be the sum of the individual current contributions of each circuit stage (each one affected with its own variation). According to these considerations, the simulation of the current consumption is simple, since each individual contribution can be obtained calculating the state of every logic gate by means of logic simulation, and then, getting the current contribution of each gate for that specific state from a library [12].

Following the previous ideas the difference of consumption between the circuit under test and the golden circuit for the test pattern j is given by:

$$\Delta I_{cut}^{j} = I_{cut}^{j} - I_{golden}^{j} =$$

$$= \sum_{i=1}^{\#gates} \{I_i^j [exp(-\frac{\triangle V_{th_{cut}}^{inter} + \triangle V_{th_i}^{intra}}{\xi v_t}) - 1]\}$$

where I_i^j is the current of typical gate i for the pattern j calculated by logic simulation. $\triangle V_{th_{cut}}^{inter}$ is generated for every die and $\triangle V_{th_i}^{intra}$ for every gate in every die.

5 Results: A Double Criterion

In order to validate the presented ideas, a simulation process has been established. The main goal was to finally emulate the experimental behaviour shown in section 2 and to study what happens when an anomaly appears into a circuit die. To better control our experiments we have prepared as example a circuit of 10,000 gates with random connections. The consumption of a typical gate was fixed to $10pA$ and the variation limits were fixed to $6\sigma_{inter} = 500mV$ for all the dice and $6\sigma_{intra} = 5mV$ for non-defective distributions. Several simulations have been carried out. The main results can be illustrated with the simulation of a set of 105 samples: 100 non-defective, 3 with alterations of their V_{th} distributions (A, B and C) and 2 with faults (D and E). The details of the defective samples are the following:

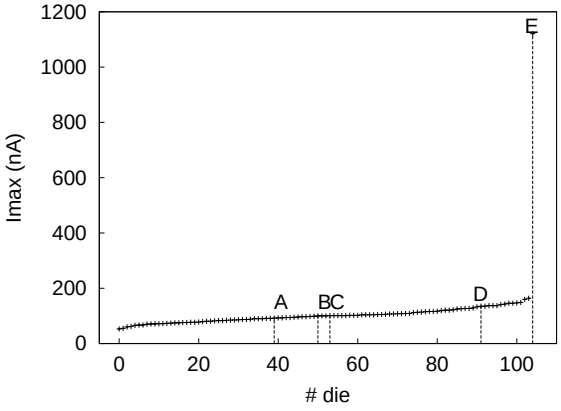

Figure 6: **Maximal currents of a simulation of 100 non-defective dice and 5 with anomalies. Only the die E is observable with a criterion of maximal current.**

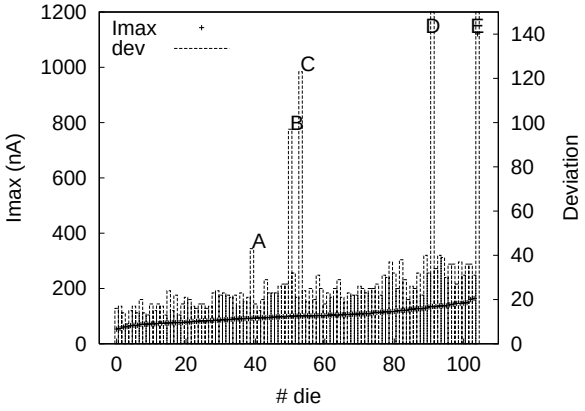

Figure 7: **Maximal currents and standard deviations of a simulation of 100 non-defective dice and 5 with anomalies. The 5 anomalous dice are observable by the double criterion.**

- *Die A*: the intra-die standard deviation, σ_{intra}, is twice bigger than the one for a non-defective distribution.
- *Die B*: the intra-die standard deviation, σ_{intra}, is four times bigger than the one for a non-defective distribution.
- *Die C*: No Normal Distribution.
- *Die D*: Small fault with small increment of current, 50% of the maximal current of a typical die. The fault controllability (probability of fault excitation) is 0.1.
- *Die E*: Fault with high increment of current, ten times the maximal current of a typical die. The fault controllability is also 0.1.

Figure 6 shows the maximal quiescent current per die in ascending order and Figure 7 adds the standard deviations of the current difference between each die and the ideal circuit (samples follow the same order than Figure 6). In Figure 6, and applying a typical I_{DDQ} testing criterion, only the die E is observable and therefore detectable. However, in Figure 7 the situation is very different, since now the 5 anomalous dice are observable. The sensitivity of the standard deviation is significantly larger than the maximal current because it is function of all the consumptions in the die and not of only one. This sensitivity increment is very important specially for deep sub-micron technologies where estimated current increments for faulty circuits are comparable to the typical consumption. Note that die D has a small fault (50% of maximal current) and can be detected as anomalous.

On the other hand, Figure 7 also shows how the deviations increase in the same way that the maximal current does (except for faulty circuits). This was also shown in Figure 4. This effect allows us to detect die A. This anomalous die presents a deviation comparable to the deviations of other dice that present bigger consumptions (bigger maximal currents). Now, the use of both criteria together, allows that this anomaly becomes observable.

In conclusion, I_{DDQ} testing quality can be increased applying a double criterion of two limits: one global, the maximal current, and another relative to a particular die, the maximal standard deviation as a function of the maximal current of that die.

Finally, we would like to underline that we have preferred to speak about current anomalies instead of current defects. I_{DDQ} testing offers a great amount of behaviour information but it is necessary to determine when an anomaly has to be considered as a defect and to adapt the new information to the compromise between defect detection and yield loss. Different applications may need different circuit quality and an anomaly that is defective for ones may be acceptable for others.

6 Conclusions and Future Work

The objective of this work has been to show that the knowledge of the current consumption behaviour of a specific circuit should be utilized for the preparation of statistical based criteria for I_{DDQ} testing, reaching better sensitivity than with the typical I_{DDQ} criterion (limit for the maximal current). I_{DDQ} is a parametric test and provides an image of the global results of the fabrication processes and the device parameters. With a small increase of the complexity of the test methodology, a great increment of the sensitivity and, therefore, of the test quality can be obtained. That is specially important in scenarios for deep sub-micron technologies and high performance products where the separation between defective and non-defective currents will diminish and will reduce the effectiveness of the I_{DDQ} testing. Statistical based criteria can be a solution.

Future works must be oriented to determine exact parameter distributions and to obtain the correlation between practical measurements and our new criterion (or other statistical based criteria).

A last point has to be considered for industrial applications. More complex criteria require more complex measurement instrumentation. Current monitors will need higher accuracy and the use of arithmetic units to calculate statistical parameters. In general, this problem can be easily faced, since current microprocessors and FPGA's allow to solve any calculation at low cost and in real time.

Acknowledgment

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